Status of Claims

Claims 1-10 are pending.

Claims 1-10 stand rejected.

Claims 1, 5, 6 and 9 have been amended by this response.

Claims 2 and 10 have been canceled and their subject matter incorporated into claims 1 and 5 respectively.

Remarks/Arguments

Claim Objections

Claims 1-10 have been objected to for containing "prentices" (understood by Applicant to mean "parenthesis") which are not related to the figures. By way of this response, claims 1 and 5 have been amended to remove any improper parenthesis.

Claims 1-2 and 5 have been objected to under 37 CFR 1.75(c) as "being in improper form because a multiple dependent claim 10." By way of this response, claim 10 has been canceled, rendering the objection thereto moot.

In view of the foregoing, Applicant respectfully requests reconsideration and withdrawal of the objections to claims 1-10.

Claim Rejections – 35 U.S.C. § 112

Claim 6 stands rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Specifically, the Action asserts that the claimed "reshaping element" is not described in the specification in such a way as to reasonably convey to one skilled in the art that the inventor was in possession

of the claimed invention at the time the application was filed. Applicant respectfully

traverses this rejection.

In response, claim 6 has been amended to recite:

The circuit of claim 5, further comprising a regeneration circuit configured to shape at the second frequency the output of the combiner.

Support for this amendment may be found, for example, in paragraphs

[0045]-[0046] and FIG. 6 of Applicant's specification as published. Accordingly,

claim 6, as amended, fully meets the requirements of 35 U.S.C. § 112, first

paragraph. Reconsideration and withdrawal of the rejection is respectfully

requested.

Claims 1-10 stand rejected under 35 U.S.C. § 112, second paragraph, as

being indefinite. Specifically, claims 1 and 5 stand rejected for reciting the terms

"relatively low" and "relatively high". By way of this response, these phrases have

been removed from the claims, rendering the rejections thereto moot.

Claims 1 and 5 have also been rejected due to an alleged lack of clarity with

regard to the phrase "combining the delayed flow with the input bit flow". The Action

goes on to state that "for the purposes of examination, the examiner will construe

the combining to occur in a multiplexer clocked at the output frequency." Applicant

respectfully objects to the Examiner's reading of additional limitations into the claim.

The term "combining" in the context of digital data processing is commonly

found in issued U.S. patent claims, and is used to represent any number of methods

for combining digital data. These methods include the use of, by way of example

only, multiplexers or logic gates. Applicant's specification supports the features

recited in present claims 1 and 5 in accordance with the requirements of 35 U.S.C.

§ 112. Reconsideration and withdrawal of the rejections of claims 1 and 5 under 35 U.S.C. § 112 is requested.

Claim 6 has been rejected for reciting the "reshaping element". As set forth above, this element has been removed from the claim, which has been amended to recite the embodiment of FIG. 6, as described in paragraph [0046] of the specification as published. Moreover, Applicant respectfully submits that one of ordinary skill in the art would immediately recognize a "regeneration circuit" or a reshaping element as a device configured to alter a characteristic of a digital data stream. These devices may be used to, for example, transcode or scale data, alter data compression and/or resolution (in the case of image data), or any number of other well-known operations regularly performed in the field of digital data processing. For at least these reasons, Applicant respectfully requests the 35 U.S.C. § 112, second paragraph, rejection of claim 6 be withdrawn.

Finally, claim 9 has been amended to remove the recitation of "and/or", rendering the rejection thereto moot.

In view of the foregoing, Applicant respectfully requests reconsideration and withdrawal of the 35 U.S.C. § 112 rejections of claims 1-10.

Claim Rejections – 35 U.S.C. § 101

Claims 1-4 stand rejected under 35 U.S.C. § 101 for failing to recite any hardware or performing a transformation on a tangible and physical article. While Applicant respectfully submits the machine-or-transformation test is not an exclusive test to determine patentable subject matter under § 101, claim 1 has been amended to recite that the step of combining the delayed and input bit streams is performed

via a computer which generates the output bit flow. Accordingly, Applicant

respectfully submits that claim 1, as amended, fully meets the requirements of 35

U.S.C. § 101.

Moreover, Applicant respectfully submits that the claimed method comprises

more than a mere abstract idea, and that neither the recitation of hardware nor the

transformation of a physical article is required to meet the requirements of 35 U.S.C.

§ 101. The Federal Circuit recently clarified the "abstract idea" exclusion for

patentable subject matter in *Research Corporation Technologies Inc. v. Microsoft*

Corp. In the case, the court found there was nothing abstract in the subject matter

of process claims directed to a digital image halftoning technique, stating:

> The invention presents functional and palpable applications in
> the field of computer technology. These inventions address "a need in
> the art for a method of and apparatus for the halftone rendering of gray
> scale images"... this court notes that inventions with specific
> applications or improvements to technologies in the marketplace are
> not likely to be so abstract that they override the statutory language
> and framework of the Patent Act.

Research Corporation Technologies Inc. v. Microsoft Corp., Fed. Cir., No. 2010-
1037, 12/8/10.

While noting the claimed methods incorporate algorithms and formulas--

usually treated as laws of nature and/or abstract ideas when standing alone, the

Federal Circuit stated they "do not bring this invention even close to abstractness

that would override the statutory categories and context." The court emphasized

that, instead of patenting a mathematical formula, the claims seek protection for a

process of halftoning in computer applications.

Similarly, Applicant submits that the claimed method of capturing, delaying,

and combining digital data streams to accelerate data flow represents a tangible

process to be performed on real data, and thus comprises much more than an

attempt to claim an abstract algorithm.

For at least the foregoing reasons, reconsideration and withdrawal of this 35

U.S.C. § 101 rejection is respectfully requested.

Claim Rejections – 35 U.S.C. § 102

Claims 1-2 and 5-10 stand rejected under 35 U.S.C. § 102(b) as being

anticipated by Ailett et al. (U.S. Patent No. 3,881,099, hereinafter Ailett). Applicant

respectfully traverses this rejection for at least the reasons set forth below.

Independent claim 1, as amended, recites:

> A method for accelerating a pseudo-random input bit flow
> having a length of 2^{n-1} bits, generated from a polynomial of an
> irreducible degree n at a first clock frequency, into an identical output
> bit flow at a second clock frequency, greater than the first clock
> frequency, the method comprising:
> collecting the output bit flow;
> delaying the collected flow by a predetermined value (τ)
> respecting the following relation:
> $$\tau = ((2^{\ell}) * T_1) - T_0.$$
> wherein T_1 represents the clock period of the input bit flow, T_0
> represents the clock period of the output bit flow, and ℓ is an integer
> setting a decimation parameter, and
> combining the delayed flow with the input bit flow in a computer
> to generate the output bit flow at the second clock frequency
> (emphasis added). [1]

Claim 1 is directed to a method for acceleration of a digital bit stream useful,

for example, in various types of communication connections or networks. The

method comprises the steps of collecting an output bit flow, delaying the collected

bit flow by a predetermined value, and combining the delayed bit flow with the input

bit flow. The delay τ applied to the collected bit flow is defined by the relationship:

$$\tau = ((2^{\ell})^* T_1) - T_0$$

wherein ℓ is an <u>integer</u>.

The Action cites Ailett as disclosing this step in its rejection of claim 2. Specifically, page 5 of the Action asserts that when ℓ is equal to .5, Ailett discloses an arrangement which meets the claimed delay relationship. The Examiner's position is incorrect. In contrast to the Examiner's articulated rationale, claim 1 requires that ℓ is an <u>integer</u>. Thus, the use of a non-integer ℓ value of <u>.5</u> does not meet the claimed limitation. For at least this reason, reconsideration and withdrawal of the 35 U.S.C. § 102 rejection of claim 1 is requested.

The above not withstanding, further independent reasons exist for the withdrawal of the present 35 U.S.C. § 102 rejection of claim 1. Ailett fails to teach, or even remotely suggest, setting a delay according to a relationship utilizing respective input and output clock periods and a decimation parameter. In fact, the cited portion of Ailett is <u>completely silent</u> as to how a delay is set, and thus cannot fairly be cited as teaching the specific relationship set forth in the claim. The mere fact that the prior art identifies a given delay period is insufficient to render obvious the claimed method of delaying the collected flow by the value of τ according to the relationship $\tau = ((2^{\ell})^* T_1) - T_0$.

Further still, the portion of Aliett cited by the Examiner in rejecting claim 2 references U.S. Patent No. 3,678,507 (Rensin). Rensin clearly teaches that the delay is set according to a half-word length (Rensin, col 2, lines 48-50), rather than by the relationship defined in claim 1. For at least these additional reasons, Applicant respectfully submits claim 1 should be allowable over the cited prior art.

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[1] Applicant notes this claim has been allowed in counterpart patent EP 1 719 248.

Claim 5 has been amended in a manner similar to claim 1, and should be allowable for at least the reasons set forth above. Claims 6-9 should be allowable at least by virtue of their ultimate dependence from claim 5. Claims 2 and 10 have been canceled, and the rejections thereto rendered moot.

In view of the foregoing, Applicant respectfully requests reconsideration and withdrawal of the 35 U.S.C. § 102(b) rejection of claims 1-2 and 5-10.

Claim Rejections – 35 U.S.C. § 103

Claims 3-4 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ailett. Applicant respectfully traverses this rejection and submits that these claims are patentable over the cited art of record for at least the reasons set forth below.

Claims 3 and 4 should be allowable at least by virtue of their dependency from claim 1. Moreover, Applicant reiterates that neither Ailett nor Rensin even remotely disclose or suggest setting a delay according to the claimed relationship, including a delay that is based on a decimation parameter.

In view of the foregoing, Applicant respectfully requests reconsideration and withdrawal of the 35 U.S.C. § 103(a) rejection of claims 3 and 4.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to
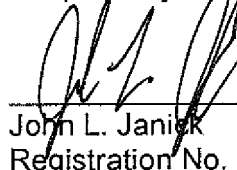
concede any issue with regard to any claim, except as specifically stated in this

paper, and the amendment of any claim does not necessarily signify concession of

unpatentability of the claim prior to its amendment.

Conclusion

Applicant believe he has addressed all outstanding grounds raised by the

Examiner and respectfully submits the present case is in condition for allowance,

early notification of which is earnestly solicited.

Should there be any questions or outstanding matters, the Examiner is

cordially invited and requested to contact Applicant's undersigned attorney at his

number listed below.

Respectfully submitted,

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